IN THE CLAIMS:

Each of the claims that remain pending and under consideration in the above-referenced application is reproduced below, in clean form, for the sake of clarity. A marked-up version of each amended claim is also enclosed herewith to clearly show each change that has been made thereto.

Please enter the claims as follows:

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1. (Twice amended) A vertical surface mount semiconductor device, comprising:

a semiconductor device having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line and having a plurality of conductive bumps secured to selected bond pads, each of said conductive bumps configured to form a conductive joint between at least one of said selected bond pads and a corresponding terminal of a substrate upon positioning said semiconductor device substantially vertically relative to said substrate.

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2. (Previously amended) The vertical surface mount semiconductor device of claim 1, wherein a conductive bump is disposed adjacent each of said plurality of bond pads.

3. The vertical surface mount semiconductor device of claim 1, further comprising a support layer.

4. The vertical surface mount semiconductor device of claim 3, wherein said support layer is disposed on another surface of said semiconductor device.

5. The vertical surface mount semiconductor device of claim 1, further comprising a support footing formed adjacent said edge.

6. The vertical surface mount semiconductor device of claim 5, wherein said support footing is disposed on another surface of said semiconductor device.

8. The vertical surface mount semiconductor device of claim 1, further comprising a laminate which connectively bonds said semiconductor device to an adjacent semiconductor device.

9. (Twice amended) A vertical surface mount semiconductor device, comprising:
a semiconductor device having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line, selected bond pads of said plurality of bond pads having conductive bumps secured thereto, said conductive bumps configured to form a joint between said selected bond pads and corresponding terminals of a carrier substrate upon substantially perpendicular orientation of said semiconductor device on said carrier substrate; and
a support member, at least a portion of which is disposed proximate said edge of said semiconductor device.

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10. The vertical surface mount semiconductor device of claim 9, wherein said support member is selected from the group consisting of support footings and support layers.

11. The vertical surface mount semiconductor device of claim 9, wherein said support member is disposed on another surface of said semiconductor device.

12. The vertical surface mount semiconductor device of claim 9, wherein a conductive bump is positioned adjacent each of said plurality of bond pads.

13. (Twice amended) A chip-on-board assembly, comprising:
a substrate with a plurality of terminals;
a semiconductor device configured to be positioned substantially perpendicularly relative to said substrate, said semiconductor device having a plurality of bond pads on a surface thereof, each of said plurality of bond pads being located adjacent an edge of said surface and arranged substantially in-line; and

electrically conductive joints configured to be secured to selected bond pads and to be disposed directly between and establish communication between selected bond pads and corresponding terminals.

14. The chip-on-board assembly of claim 13, wherein each of said plurality of bond pads has an electrically conductive joint disposed adjacent thereto.

15. (Previously amended) The chip-on-board assembly of claim 13, further comprising a support member in contact with at least one of said semiconductor device and said substrate.

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16. The chip-on-board assembly of claim 15, wherein said support member is selected from the group consisting of support footings and support layers.

17. The chip-on-board assembly of claim 15, wherein said support member is disposed proximate said edge of said semiconductor device.

18. The chip-on-board assembly of claim 13, wherein said semiconductor device is laminated to an adjacent semiconductor device.

19. (Twice amended) A computer including a vertically mountable semiconductor device, the semiconductor device comprising:

a semiconductor die with a plurality of circuit traces and a plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof in a substantially in-line arrangement, each of said plurality of bond pads communicating with one of said plurality of circuit traces; and

conductive bumps secured to selected bond pads, said conductive bumps each configured to form a joint between one of said selected bond pads and a corresponding terminal of a substrate

when said semiconductor device is positioned substantially perpendicularly relative to said substrate.

20. The computer of claim 19, wherein each of said plurality of bond pads has a conductive bump in communication therewith.

21. The computer of claim 19, wherein said semiconductor device further comprises a support member.

22. The computer of claim 21, wherein said support member is selected from the group consisting of support footings and support layers.

23. The computer of claim 21, wherein said support member is disposed proximate said edge.

24. The computer of claim 19, wherein said semiconductor device is laminated to an adjacent semiconductor device.